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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/160,824	09/25/1998	TSIU CHAN	97-C-108	6763

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/160,824	CHAN ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-16,18 and 19* is/are rejected.

7)☒ Claim(s) *7,8, and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Declaration under 37 CFR 1.131

2. The declaration filed on 08/25/03 under 37 CFR 1.131 has been considered but is ineffective to overcome either the KANEKO (6,255,736) reference or the WENZEL et al. (6,150,724) reference.

A. The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the WENZEL et al. (6,150,724) reference to either a constructive reduction to practice or an actual reduction to practice. Firstly, applicants offer no proof of actual reduction to practice other than the statement "Upon information and belief, the invention in this application was reduced to practice before March 2, 1998..." This statement does not carry enough weight to establish reduction to practice because the preamble "Upon information and belief," in-

forms the reader that applicants were not present at the reduction but believe it happened because unnamed parties told them about it. Applicants' beliefs carry insufficient weight. Secondly, applicants' only evidence of diligence it that they tarried only six months after the effective date of WENZEL et al. to file their own application. This evidence lacks weight, as there is no explanation of what activities, over the six-month period, caused applicants to lack the time to make their own application.

B. The evidence submitted is insufficient to establish a conception of the invention claimed in claims 6-19 prior to the effective date of the either the KANEKO (6,255,736) reference or the WENZEL et al. (6,150,724) reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897).

Claims 6-12 all require at least a first metal region projecting from the active face of a first integrated circuit chip overlain by at least a second metal region projecting from a surface of a second integrated circuit chip. Applicants have provided proof they conceived of a device having a first integrated circuit chip (IC1, or "mother chip," as it is referred to in the Invention Disclosure Form accompanying applicants affidavit) and a second integrated circuit chip (IC2, "daughter chip"). Arguably the "posting structure to allow contact of pad openings" is the claimed "at least one

metal region projecting from a surface of the second integrated circuit chip." However, there is no evidence that applicants conceived of this "posting structure" to exist anywhere except on the second, or "daughter" chip. Hence there is no evidence of conception of the claimed combination of the "first metal region projecting from the active face of a first integrated circuit chip," with the other elements of claim 6.

Claims 13-19 all require a "bonding layer" between the chips. Applicants' Invention Disclosure Form simply does not disclose any such thing.

Briefly put, applicants' Invention Disclosure Form discloses subcombinations of the combinations claimed in claim 6 and claim 13 but the Invention Disclosure Form does not disclose the entire claimed combinations.

Election/Restriction

3. Applicant's election without traverse of Group I, claims 1-19 in Paper No. 4 is acknowledged.

Priority

4. Applicants have made no claim for priority.

Oath/Declaration

5. The oath/declaration filed on 09/25/98 is acceptable.

Drawings

6. The drawings are objected to by the PTO Draftsperson for the reasons noted on the Notice of Draftsperson's Patent Drawing Review, form PTO-948, attached to Paper #5, which was mailed 10/24/01.

Priority

7. Applicants have made no claim for priority.

Information Disclosure Statement

8. The Information Disclosure Statement filed on 05/26/99 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1,3,6,9,11,12,13,14, and 19 rejected under 35 U.S.C. 102(e) as being anticipated by KANEKO (6,255,736).

Kaneko discloses a microprocessor comprising a first chip, or integrated circuit chip 11, having an active face including a central processing unit 41; and a second chip, or integrated circuit chip 12, having an active face, the second chip 12 mounted on, and electrically connected to, the active face of the first chip, further comprising at least one metal region 20 projecting from the active face of the first integrated circuit chip 11, at least one metal region 21 projecting from a surface of the second integrated circuit chip 12, the metal regions further comprising: conductive regions projecting from the active faces of the first 11 and second 12 chips (note that only one alternate structure of claim 14 need be present), and at least two groups of contact pads 13 on the active surface of the first integrated circuit chip 11 for external connection to the central processing unit 41, wherein the second chip 12, or integrated circuit chip 12, adds functionality, or provides added functionality, to the central processing unit 41 of the first chip 11, wherein the electrical connection is by a bonding layer 20A between the metal regions 20 and 21 on the active faces of the first 11 and second 12 chips, wherein an active face of the second integrated circuit chip 12 faces the active face of the first integrated circuit chip 11, wherein the at least one metal region 20 projecting from the active face of the first integrated circuit chip 11 overlies the at least one metal region 21 projecting from a surface of the second integrated circuit chip 12, wherein the electrical connection between the first

integrated circuit chip 11 and the second integrated circuit chip 12 is by direct connection of metal regions 20 and 21 on the active faces of the first 11 and second 12 integrated circuit chips by a bonding layer 20A, wherein a length and width of the second integrated circuit chip 12 are less than a respective length and width of the first integrated circuit chip 11, and wherein a width of the second integrated circuit chip 12 is less than a width of the first integrated circuit chip 11, and is less than a distance between the two groups of contact pads 13, and wherein the active regions of the first 11 and second 12 chips are spaced apart by the metal regions 20 and 21. Note figures 5A, 5B, and 7 and column 6 lines 60-67, column 7 line 66-67, and column 8 lines 1-9 of Kaneko

B. Claims 1-6,9-11,13,15,16,18, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by WENZEL et al. (6,150,724).

Wenzel et al. discloses a microprocessor comprising a first chip 102, or integrated circuit chip, having an active face including a central processing unit; and a second chip 104, or integrated circuit chip, having an active face, the second chip 104 mounted on, and electrically connected to, the active face of the first chip 102, further comprising a third chip (not shown, see figure 8 and column 6 lines 47-59) or integrated circuit chip mounted on, and electrically connected to, the active face of the first chip 102 or integrated circuit chip adjacent the second chip 104 and at least two groups of contact pads 208 on the active surface of the first integrated circuit chip 102 for external connection to the central processing unit, wherein the second

chip 104, or integrated circuit chip, adds functionality, or provides added functionality, to the central processing unit of the first chip 102 and the third chip adds further functionality to the central processing unit of the first chip 102 or integrated circuit, wherein the electrical connection is by a bonding layer 312 between metal regions 210 and 310 projecting from the active faces of the first 102 and second 104 chips, wherein the electrical connection between the first integrated circuit chip 102 and the second integrated circuit chip 104 is by direct connection of the metal regions 210 and 310 projecting from the active faces of the first 102 and second 104 integrated circuit chips by a bonding layer 312, wherein an active face of the second integrated circuit chip 104 faces the active face of the first integrated circuit chip 102, wherein the metal region 210 projecting from the active face of the first integrated circuit chip 102 overlies the metal region 310 projecting from a surface of the second integrated circuit chip 104, wherein the second integrated circuit chip 104 has a width less than a distance between the two groups of contact pads 208, and wherein a width of the second integrated circuit chip 104 is less than a width of the first integrated circuit chip 102, and wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array, and the second integrated circuit chip 104 comprises one of a cache memory, a dynamic random access memory (DRAM), a static random access memory (SRAM), and a flash memory, and an analog-to-digital converter.

Note figures 5 and 14 and column 6 lines 47-53 and 60-67 and column 7 lines 1-17 of Wenzel et al. With respect to the CPU/DSP/A-D/cache/DRAM/SRAM/flash limitations, note that in column 6 spanning to column 7, Wenzel et al. state that

> Generally, the structure of FIG. 5 may be used to integrate any one integrated circuit device with one or more other integrated circuit device(s) either made by the same process or different processes. For example, one of either the chip 102 or chip 104 may be a digital signal processor (DSP), a microcontroller (MCU), a general purpose microprocessor or computer central processing unit (CPU), an analog-to-digital (A/D) converter, a digital-to-analog (D/A) converter, any memory device (such as a DRAM, an static random access memory (SRAM), an electrically programmable read only memory (EPROM), an EEPROM, a ferroelectric memory, a nonvolatile memory, a read only memory (ROM), ferromagnetic memory, optical storage, or the like), bipolar device, power metal on semiconductor field effect transistor (MOSFET) devices, radio frequency (RF) devices, infrared (IF) devices, analog or digital devices, sensors, discrete devices, micromachined devices, application specific integrated circuits (ASICs), telecommunications ICs, III-V devices, oscillators, liquid crystal display (LCD) displays, **or any other device typically made in integrated circuit or electrical circuit form, while the other device 102 or 104 may be any one of the same**. In a preferred form, one of the devices 102 or 104 will be some execution unit, such as a microprocessor CPU, while the other device of 102 or 104 will be some memory structure which functions as local memory for the CPU (e.g., a cache or embedded memory).

C. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by ISOMURA et al. (5,477,067).

Isomura et al. discloses a microprocessor comprising a first integrated circuit chip 304 having an active face including a central processing unit comprising a digital signal processor, and a second integrated circuit chip 303 mounted on, and electrically connected to, the active face of the first integrated circuit, wherein the second integrated circuit chip provides added functionality to the central processing unit of the first integrated circuit, an active face of the second integrated circuit chip faces the active face of the first integrated circuit chip, and the second integrated circuit chip comprises a memory, being either a dynamic random access memory (DRAM)

or a static random access memory (SRAM). Note figures 3Q, 3R, and 3S and column 17 lines 1-36 of Isomura et al.

It is the examiner's current position that applicants have failed to show diligence required to overcome, by affidavit, the 102(e) rejection of claims 1-5 as anticipated by WENZEL et al. However, in the interests of compact prosecution the statutory bar evidenced by Isomura et al. is made of record at this time.

Allowable Subject Matter

Claims 7,8,and 17 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. After February 4, 2004, this telephone number will change to (571) 272-1913. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
12/2003

Minhloan Tran
Primary Examiner
Art Unit 2826